DISPLAY DEVICE AND METHOD OF MEASURING CONTACT RESISTANCE THEREOF

[0001] This application claims the benefit of Korean Patent Application No. 10-2015-0131843 filed on Sep. 17, 2015, the entire contents of which is incorporated herein by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention

[0003] The present disclosure relates to a display device and a method for measuring contact resistance thereof.

[0004] Discussion of the Related Art

[0005] Various flat panel display devices such as a liquid crystal display (LCD), an organic light emitting display device, a plasma display panel (PDP), an electrophoretic display (EPD), and the like, have been developed.

[0006] An LCD displays an image by controlling an electric field applied to liquid crystal molecules according to a data voltage. An active matrix type LCD has thin film transistors (TFTs) formed in every pixel.

[0007] A process of manufacturing an LCD includes a substrate cleaning process, a substrate patterning process, an alignment film forming/rubbing process, a substrate bonding and liquid crystal dropping process, a driving circuit mounting process, an inspection process, a repair processing, a liquid crystal assembly process, and the like.

[0008] During the substrate cleaning process, foreign materials contaminating surfaces of an upper glass substrate and a lower glass substrate of a display panel are removed with a cleaning solution. During the substrate patterning process, signal lines including a data line and a gate line, a thin film transistor (TFT), a pixel electrode, a common electrode, and the like, are formed on the lower glass substrate. Also, during the substrate patterning process, a black matrix, a color filter, and the like, are formed on the upper glass substrate. During the alignment film forming/rubbing process, an alignment film is coated on each of the glass substrates and rubbed with rubbing cloth or photo-aligned. Through the sequential processes, data lines to which a video data voltage is supplied, gate lines intersecting with the data lines, to which a scan signal, i.e., a gate pulse, is sequentially supplied, and a TFT array including TFTs formed at intersections of the data lines and the gate lines, pixel electrodes connected to the TFTs, a storage capacitor, and the like, are formed on the lower glass substrate. The common electrode is formed on the upper glass substrate in a vertical field driving mode such as a twisted nematic (TN) mode and a vertical alignment (VA) mode and formed on the lower glass substrate together with a pixel electrode in an in-plane field driving mode such as an in-plane switching (IPS) mode or a fringe field switching (FFS) mode. A polarizer is adhered to each of the upper glass substrate and the lower glass substrate.

[0009] During the substrate bonding and liquid dropping process, a sealant is drawn on any one of the upper and lower glass substrates of the display panel, liquid crystal is dropped, and thereafter, the upper glass substrate and the lower glass substrate are bonded with the sealant. A liquid crystal layer is defined as a liquid crystal region defined by the sealant.

[0010] During the driving circuit mounting process, a drive integrated circuit (IC) in which driving circuits are integrated is adhered to data pads of the display panel by an anisotropic conductive film (ACF) through a chip-on-glass (COG) bonding or a tape automated bonding (TAB) process. A gate driving circuit may be directly formed on the lower glass substrate through a gate-in-panel (GIP) process or may be adhered to gate pads of the display panel by an ACF in a tape automated bonding (TAB) process during the driving circuit mounting process. Also, during the driving circuit mounting process, ICs and printed circuit board (PCB) are connected by a flexible circuit board such as a flexible printed circuit board (FPCB), a flexible flat cable (FFC), and the like.

[0011] The inspection process includes inspection of a driving circuit, inspection of a line such as a data line and a gate line formed on a TFT array substrate, inspection performed after formation of a pixel electrode, electrical inspection performed after the substrate bonding and liquid crystal dropping process, inspection of lighting, and the like. The inspection process may include a process (hereinafter, referred to as a "bonding resistance inspection method) of inspecting contact resistance between a drive IC and the substrates of the display panel in the COG bonding process. During the repair process, a defect discovered during the inspection process is repaired.

[0012] When the display panel is completed through the aforementioned sequential processes, a process of assembling a liquid crystal module is performed. During the process of assembling a liquid crystal module, a backlight unit is aligned below the display panel and the display panel and the backlight unit are assembled using a device such as a guide/case member, or the like.

[0013] During the COG bonding process, an ACF is aligned on a substrate SUBS, and a drive IC DIC is aligned above the ACF. Bumps BUMP of the drive IC DIC face pads PAD formed on the substrate SUBS with the ACF interposed therebetween. Thereafter, the substrate SUBS is heated and the drive IC DIC is pressed and heated such that the bumps BUMP of the drive IC DIC are adhered to the pads PAD on the substrate SUBS. Here, conductive particles CP of the ACF electrically connect the bumps BUMP of the drive IC DIC and the pads PAD of the substrate SUBS. The pads PAD are connected to signal lines formed on the substrate SUBS. The drive IC DIC outputs an output signal through the bumps BUMP, and the output signal is supplied to the signal lines of the substrate SUBS through the pads.

[0014] Contact resistance between the bumps BUMP of the drive IC DIC and the pads PAD of the substrate SUBS adhered during the COG bonding process is also known as bonding resistance. A bonding resistance inspection method is essentially performed during the COG bonding process. High contact resistance indicates a defect COG bonding process, and thus, the drive IC DIC should be removed and bonded again. In order to perform bonding resistance inspection method, a dummy pad for resistant measurement connected to the pads on the substrate SUBS is separately provided. The bonding resistance inspection method is performed as a manual measurement method in such a manner that an inspector directly connects a terminal of a measurement instrument to the dummy pad for resistance measurement to perform measurement.

SUMMARY OF THE INVENTION

[0015] The related art bonding resistance inspection method has the following problems.